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10/693,568

PATENT
Conf. No.: 1995

IN THE UNITED STATES PATENT OFFICE

Applicants: Patrick Lysaght et al.
Assignee: Xilinx, Inc.
Title: Method and Apparatus for Power Optimization During an Integrated Circuit Design Process
Serial No.: 10/693,568 File Date: 10/24/2003
Examiner: Naum B. Levin Art Unit: 2825
Docket No.: X-1374 US Conf. No.: 1995

Mail Stop AMENDMENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO FIRST OFFICE ACTION

Dear Sir:

In response to the First Office Action mailed from the Patent Office on August 11, 2005, Applicants make the following remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.